REMARKS

In paragraph 2 of the Office action, claims 1-13 and 31-41 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable "over claims 1–30 of copending Application No. 10/689,258 ." Serial number 10/689,**258** is directed to a Method for Producing Single Walled Carbon Nanotubes and is completely unrelated to the subject matter of the instant disclosure. It is believed that the examiner intended to cite copending Application No. 10/689,**256.** This was brought to the examiner's attention in the last amendment filed September 13, 2007, but the examiner has reiterated the double patenting rejection based on Application No. 10/689,**258.** Clarification is respectfully requested. Furthermore, it is noted that a number of claims have been cancelled from copending Application No. 10/689,**256** and the claims of instant application amended such that the examiner is respectfully requested to determine if the double patenting rejection is still proper.

In paragraph 4 of the Office action, claims 1-13 and 31-41 stand rejected under 35 U.S.C. § 101 "because the claimed invention is directed to non-statutory subject matter." Claim 1 was substantially amended in the last response and is again substantially amended in the current response. Claim 1 has been amended such that claim 1 is now limited to determining a dimensional extrema instead of determining a global extrema. Claim 1 is further amended to recite serially outputting in bursts, the least and most significant bytes of the local extrema, with the length of the bursts selected to optimize use of each processing element's ALU. Support for that amendment is found, for example, in paragraph [0068] of the application as published which provides:

> [0068] It should further be noted that the order in which the LS-bytes and the MS-bytes are placed onto the transfer network and the number of PEs to which the bytes are transferred to may be altered while remaining within the scope of the present invention. For example in the current embodiment, the LS and MS bytes are transferred in bursts. The burst length may be selected to approximately equalize the number of lost transfer cycles and the number of lost ALU cycles. This effectively reduces the number of lost transfer cycles as compared to the first approach discussed above. Additionally by using bursts, the ALU can start comparing shorts more quickly as compared to the second approach discussed above, thus reducing the number of lost processing cycles. Once the ALU is started, the use of bursts helps to minimize the time that the ALU is required to wait for data.

The examiner explains on page 3 of the Office action that the "claimed invention merely involves calculations and manipulations of data among the processors to compute an extrema for a plurality of values." Claim 1 recites:

> A method of operating an n-dimensional array of processing elements to determine a dimensional extrema for a plurality of values stored in said n-dimensional array of processing elements, the method comprising:
>
> determining a local extrema for each of said processing elements, said local extrema having a most significant byte and a least significant byte;
>
> **serially outputting in bursts** said most significant bytes and said least significant bytes of said local extrema from each of said processing elements to a neighboring processing element until every processing element in a first dimension has received all local extrema along said first dimension, **wherein a burst length is selected to optimize use of each processing element's ALU**;
>
> determining within each of said processing elements a first dimensional extrema for said first dimension of said n-dimensional array, wherein said first dimensional extrema is determined from a plurality of local extrema most significant bytes and least significant bytes stored in said processing elements in said first dimension and wherein said first dimensional extrema has a most significant byte and a least significant byte; and
>
> saving said dimensional extrema.

As seen, claim 1 not only recites steps that are directed to the calculation and manipulation of data, but also recites subject matter that is directed to the movement of data in bursts of a length selected to optimize the use of each processing element's ALU. The highlighted language is significant because it enables the process of optimizing the operation of an n-dimensional array of processing elements. Applicant is not attempting to patent the calculation of a dimensional extrema, but rather is attempting to patent a particular process of optimizing the operation of an n-dimensional array of processing elements to calculate a dimensional extrema. The claims, if granted, would not preempt all methods of calculating a dimensional extrema, only the particular optimized method set forth in the claims.

The examiner explains on page 3 of the Office action:

> The inputs are numbers and the output is also a number. The extrema produce[d] by the claimed invention is not a real world result but merely a numerical value without a practical application recited in the claims that makes the result useful, concrete and tangible. (emphasis added)

Simply because the final result is a number does not mean that the claim is not directed to a useful, concrete, and tangible result. Optimizing the operation of an n-dimensional array of processing elements is certainly a useful exercise. The claimed optimization process is reproducible and thus concrete. The result is tangible because it enables the n-dimensional array of processing elements to operate in an efficient manner, which is a real world result.

In view of the examiner's comments, the examiner appears to believe that, for a claimed invention to achieve a "tangible result," a practical application *must be recited as one of the elements of the claim.* Such a test is improper and contrary to legal precedent. The Interim Guidelines state, "[T]o be eligible for patent protection the claimed invention *as a whole must accomplish* a practical application. That is, *it must produce* a 'useful, concrete and tangible result.'" (Interim Guidelines of 22 November 2005, first paragraph, citing *State Street Bank & Trust Co. v. Signature Financial Group, Inc.*, 149 F.3d 1368 at 1373-74 (Fed. Cir. 1998), emphasis added.) The Interim Guidelines also indicate that "[T]he focus is . . . on whether the *final result achieved* by the claimed invention is 'useful, tangible, and concrete'" (MPEP 2106 (IV)(C)(2), emphasis added). The examiner appears to have understood the words "accomplish," "produce," and "achieved" from the Interim Guidelines to mean that the claim must *recite* a tangible result as one of the elements of the claims and appears to have ignored the directive that the *claimed invention as a whole* be considered. That approach is simply incorrect.

Legal precedent makes clear that the examiner is applying an improper analysis. For example, in *In re Alappat*, 33 F.3d 1526 (Fed. Cir. 1994), the Federal Circuit reversed a decision by the Board of Patent Appeals and Interferences ("the Board") and held that Alappat's claimed invention to a rasterizer for converting vector list data representing sample magnitudes of an input waveform into anti-aliased pixel illumination intensity data to be displayed on a display means was indeed statutory under 35 U.S.C. § 101. Even though the claim at issue (claim 15) was directed to a machine, the Board argued that the claimed subject matter fell within a judicial exception as being directed to elements that merely carried out a mathematical algorithm. (*Id.* at 1542.) The Federal Circuit rejected that contention, noting that claim 15 was directed to a combination of elements for performing a combination of calculations "to transform, i.e., rastorize, digitized waveforms (data) into anti-aliased, pixel illumination data *to produce a smooth waveform.*" (*Id.* at 1544, emphasis added.) Importantly, the claim at issue *did not recite the result of "a smooth waveform,"* yet the court understood that the claimed invention as a

whole produced that result in light of the description of the invention being claimed. Indeed, the Federal Circuit in *AT&T Corp. v. Excel Communications, Inc.*, 172 F.3d 1352 (Fed. Cir. 1999) explicitly commented on this aspect of *Alappat* in stating, "In *Alappat*, we held that more than an abstract idea was claimed because the claimed invention as a whole was directed toward forming a specific machine *that produced the useful, concrete, and tangible result of a smooth waveform display.*" (*Id.* at. 1357.) Again, *the claim did not recite the result of producing or displaying "a smooth waveform."* Thus, the examiner's failure to look beyond the explicit claim language for what the claimed invention as a whole achieves and the examiner's apparent requirement in the present instance that the claims themselves should recite a tangible result as one of the elements is contrary to legal precedent.

Should the examiner think that *Alappat* is distinguishable from the present matter simply because the claims at issue in *Alappat* were apparatus claims whereas certain of the present claims at issue are method claims, it is respectfully pointed out that the Federal Circuit has already spoken to the contrary. For example, in *AT&T*, the Federal Circuit stated:

> Whether stated implicitly or explicitly, *we consider the scope of § 101 to be the same regardless of the form - machine or process - in which a particular claim is drafted.* See, e.g., *In re Alappat*, 33 F.3d at 1581, 31 USPQ2d at 1589 (Rader, J., concurring) ("Judge Rich, with whom I fully concur, reads Alappat's application as claiming a machine. In fact, *whether the invention is a process or a machine is irrelevant.* The language of the Patent Act itself, as well as Supreme Court rulings, clarifies that Alappat's invention fits comfortably within 35 U.S.C. § 101 whether viewed as a process or a machine."); State Street, 149 F.3d at 1372, 47 USPQ2d at 1600 ("[F]or the purposes of a § 101 analysis, *it is of little relevance whether claim 1 is directed to a 'machine' or a 'process,'....*"). Furthermore, the Supreme Court's decisions in *Diehr*, *Benson*, and *Flook*, all of which involved method (i.e., process) claims, have provided and supported the principles which we apply to both machine-- and process-type claims. Thus, *we are comfortable in applying our reasoning in Alappat and State Street to the method claims at issue in this case.* (172 F.3d at 1357-58, emphasis added.)

Accordingly, the insights from the Federal Circuit's analysis in *Alappat* are indeed relevant to the matter at hand.

As further evidence that the claims currently presented are directed to a statutory process, the examiner's attention is respectfully directed to the following patents. Although the issuance of patents in other cases is not binding on the examiner, the issuance of these patents indicates that the current claims fall within the bounds of allowable subject matter. The issuance of these

patents is not "irrelevant to the rejection" as asserted by the examiner because the Office has the obligation to uniformly apply the rules related to patentable subject matter. The issuance of these patents without an explanation of how the instant claims are distinguishable from the allowed claims of these patents indicates that the Office is not applying the rules related to patentable subject matter in a uniform manner.

U.S. Patent No. 5,710,732 is entitled Calculating the Average of Four Integer Numbers Rounded Away From Zero in a Single Instruction Cycle. Claim 1 reads:

> 1. A method of operating a circuit to obtain an average of four unsigned operands, such that the average is an integer rounded away from zero, comprising:
>
> appending two zero's to a left end of each of the operands to provide extended operands;
>
> summing the extended operands to provide an intermediate result;
>
> removing a lowest significant bit and a second lowest significant bit from the intermediate result to provide a shortened intermediate result;
>
> incrementing the shortened intermediate result to provide the average when the removed second lowest significant bit is a one; and
>
> providing the shortened intermediate result as the average when the removed second lowest significant bit is a zero.

U.S. Patent No. 5,751,617 is entitled Calculating the Average of Two Integer Numbers Rounded Away From Zero in a Single Instruction Cycle. Claim 1 reads:

> 1. A method of operating a circuit to obtain an average of two unsigned operands such that the average is an integer rounded away from zero in a single instruction cycle, comprising:
>
> logically right-shifting each of the operands by one bit position, wherein bits in a lowest significant bit position of the operands become shifted-out bits;
>
> summing the right-shifted operands to obtain a result; and
>
> incrementing the result when any of the shifted-out bits is a one.

U.S. Patent No. 5,835,389 is entitled Calculating the Absolute Difference of Two Integer Numbers in a Single Instruction Cycle. Claim 1 reads:

> 1. A method of operating a circuit to obtain an absolute difference of first and second unsigned integer operands, such that the absolute difference is an unsigned integer, comprising:
>
> bit-complementing the second operand;
>
> summing the first and bit-complemented second operands to obtain an intermediate result;
>
> incrementing the intermediate result to obtain an incremented intermediate result;
>
> bit-complementing the intermediate result to obtain a bit-complemented intermediate result;
>
> determining whether the intermediate result overflows provided the first and bit-complemented second operands and the intermediate result are considered unsigned numbers;
>
> selecting the incremented intermediate result to obtain the unsigned absolute difference when the overflow occurs; and
>
> selecting the bit-complemented intermediate result to obtain the unsigned absolute difference when the overflow does not occur.

U.S. Patent No. 5,917,739 is entitled Calculating the Average of Four Integer Numbers Rounded Towards Zero in a Single Instruction Cycle. Claim 1 reads:

> 1. A method of operating a circuit to obtain an average of four signed operands, such that the average is an integer rounded towards zero in a single instruction cycle, comprising:
>
> appending two bits to a left end of each of the operands to provide extended operands, wherein for each operand the two appended bits are zero's when the operand is a positive number, and one's when the operand is a negative number,
>
> summing the extended operands to provide an intermediate result;
>
> removing a lowest significant bit and a second lowest significant bit from the intermediate result to provide a shortened intermediate result;
>
> incrementing the shortened intermediate result to provide the average when the intermediate result has a negative value and either of the removed bits is a one; and

providing the shortened intermediate result as the average (i) when the intermediate result has a positive value, and (ii) when the intermediate result has a negative value and both of the removed bits are zero's.

U.S. Patent No. 6,007,232 is entitled Calculating the Average of Two Integer Numbers Rounded Towards Zero in a Single Instruction Cycle. Claim 1 reads:

1. A method of operating a circuit to obtain an average of two unsigned operands such that the average is an integer rounded towards zero in a single instruction cycle, comprising:

logically right-shifting each of the operands by one bit position, wherein bits in a lowest significant bit position of the operands become shifted-out bits;

summing the right-shifted operands to obtain a result; and

incrementing the result when both of the shifted-out bits are one's.

Claim 31 is an apparatus claim directed to an n-dimensional array of processing elements and therefore also falls within the statutory definition of patentable subject matter. See, for example, U.S. Patent No. 7,031,996 entitled Calculating Square Root of Binary Numbers with Fixed-Point Microprocessor. Claim 1 provides:

1. A square root calculator comprising:
a binary searching module operable to accept a number, perform a binary search operation, and return an integer portion of the square root of the number;
a fraction calculating module operable to calculate a fractional portion of the square root; and a summing module operable to sum the integer portion and the fractional portion to obtain the square root.

Finally, applicant asserts that the method of claim 1 and the apparatus of claim 31 are no different in principle from methods and apparatus for generating random numbers. It could be argued that random numbers not applied to a specific problem do not represent anything in the real world, yet the Office routinely grants patents containing method and apparatus claims that do no more than generate random numbers. The following represents but a small sample of the hundreds of such patents routinely granted that recite either a process, an apparatus, or both, for generating random numbers:

7,233,965	Continuous Random Number Generation Method and Apparatus	Issued June 19, 2007
7,197,523	Efficient Use of Detectors for Random Number Generation	Issued March 17, 2007
7,188,131	Random Number Generator	Issued March 6, 2007
7,176,882	True Random Number Generation	Issued January 23, 2007

In view of the foregoing, it is believed that the 35 U.S.C. § 101 rejection in the last Office action has been overcome and should now be withdrawn.

Request for Interview

Applicant has made a diligent effort to place the instant application in condition for allowance. If the examiner is of the opinion that the instant application is in condition for disposition other than through allowance, the examiner is respectfully requested to contact applicant's attorney at the telephone number listed below **so that an interview may be scheduled before the issuance of a final Office action.**

Respectfully submitted,

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